Amendments to the Specification

Please replace the paragraph beginning at page 8, lines 5-30, with the following amended paragraph:

Referring now to Figure 2 as well the preceding figure, each of the 64 processors in the module includes a control store 30, which in this illustrative embodiment is 256 steps deep with 96 bits wide processor control codes that determine the logic function of the associated processor 31 during that step in the emulation process. As will be appreciated by those skilled in the art, in carrying out an emulation, a compiler program compiles the logic design as a series of processor instruction steps that are stored in the control store 30 of each processor in a module. In accordance with the teaching of this invention, in order to allow reading and/or writing to the RAM memories of a module, the control store program in one of the control store memories 30 is compiled so that it has a bit in a bit location that is decoded as command to memory controller 22 to disable all module processors from writing to or reading from the module RAM memories 18. As illustrated in Figure 2, bit "M" in step "N" is set to a predetermined binary value ("0" or "1"), decoder 33 decodes the state of bit "M" in step "N" and sends a disable command to memory controller 22 over the maintenance bus. This allows work station 22 to transfer data to or from the module's RAM memories 18 during this step in each cycle of control store 30. When the program progresses to the next step, the disable command terminates and the processors are again enabled for data transfer to and from the RAMs. Of course, the program cold be compiled and decoded to provide two or more interrupts each cycle of the control store.